Heiner Litz

Curriculum Vitae

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Address: Department of Computer Engineering
1156 High St, Santa Cruz, CA 95064
Email: heiner.litz@gmail.com
WWW: https://people.ucsc.edu/~hlitz/

Overview

I am working on computer architecture and systems to design next-generation microprocessors for scale-out data centers. My current interests evolve around redesiging the processor frontend (Icache, BTB, branch predictor, uop cache) and the memory system, to address large footprint warehouse-scale computing workloads. I design new microarchitecture mechanisms while leveraging profile-guided optimization, compiler and machine learning techniques to develop hollistic hardware-software co-designed solutions. I am building full stack prototypes including applications, firmware, FPGAs, ASICs and have contributed to the Linux kernel. I am currently advising 9 Ph.D. students and my research is supported by grants totalling $2.9M from the National Science Foundation (NSF), Samsung, Google, Facebook, Intel, Western Digital, Broadcom and NXP.

Work Experience

2018-	Assistant Professor at the University of California, Santa Cruz
2018-2020	Consulting Researcher at Google, Mountain View
2017	Visiting Faculty at Google, Mountain View
2015-2016	Lecturer and Postdoctoral Researcher, Stanford University, with Prof. C. Kozyrakis
2012-2015	Postdoctoral Researcher, Stanford University, with Prof. D. Cheriton
2008	Hardware Engineering Intern, SUN Microsystems
2006-2012	Research Assistant, University of Heidelberg and Mannheim University

Education

2015	Postdoc in Electrical Engineering, Stanford University *Advisor*: David Cheriton and Christos Kozyrakis
2011	PhD. in Computer Engineering, Mannheim University *Advisor*: Professor Ulrich Bruening
2010	Visiting Researcher, University of Valencia *Advisor*: Professor Jose Duato
2006	Diplom Informatik (M.Sc), Mannheim University

Honors and Awards

- Intel Outstanding Researcher Award '21
- NSF CAREER Award
- IEEE MICRO Top Pick of 2019 Award
- Memorable Paper Award, NVMW'17
- Dissertation with honors, Summa Cum Laude
- Best paper award, ARC'09
- Best paper award, ICPP'08

Teaching Experience

Instructor, CSE120: "Computer Architecture"	'21, '20, '19, '18
Instructor, CSE226: "Advanced Parallel Computing"	'21, '20, '19
Instructor, CSE125: "Logic Design with Verilog"	'21, '20, '19

Publications

Selected Publications

1. Litz, H., G. Ayers, and P. Ranganathan (2022). CRISP: Critical Slice Prefetching. In: *Proceedings of the Twenty-Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'22)*.
2. Khan, T. A., D. Zhang, A. Sriraman, J. Devietti, G. Pokam, H. Litz, and B. Kasikci (2021). Ripple: Profile-Guided Instruction Cache Replacement for Data Center Applications. In: *Proceedings of the 48th International Symposium on Computer Architecture (ISCA'21)*.
3. Ayers, G., H. Litz, C. Kozyrakis, and P. Ranganathan (2020). Classifying Memory Access Patterns for Prefetching. In: *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'20)*, pp.513–526.
4. Khan, T. A., A. Sriraman, J. Devietti, G. Pokam, H. Litz, and B. Kasikci (2020). I-SPY: Context-Driven Conditional Instruction Prefetching with Coalescing. In: *Proceedings of the 53nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'20)*.
5. Ayers, G., N. P. Nagendra, D. I. August, H. K. Cho, S. Kanev, C. Kozyrakis, T. Krishnamurthy, H. Litz, T. Moseley, and P. Ranganathan (2019). AsmDB: understanding and mitigating front-end stalls in warehouse-scale computers. In: *Proceedings of the 46th International Symposium on Computer Architecture (ISCA'19)*.
6. Ni, Y., J. Zhao, H. Litz, D. Bittman, and E. L. Miller (2019). SSP: Eliminating Redundant Writes in Failure-Atomic NVRAMs via Shadow Sub-Paging. In: *Proceedings of the 52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'19)*.
7. Litz, H., A. Klimovic, and C. Kozyrakis (2017). ReFlex: Remote Flash == Local Flash. In: *22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'17)*.
8. Litz, H., D. Cheriton, A. Firoozshahian, O. Azizi, and J. P. Stevenson (2014). SI-TM: reducing transactional memory abort rates through snapshot isolation. In: *19th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'14)*.

Journal Papers

1. Litz, H., J. Gonzalez, A. Klimovic, and C. Kozyrakis (2021). RAIL: Predictable, Low Tail Latency for NVMe Flash. In: *Proceedings of ACM Transactions on Storage (TOS)*.
2. Nagendra, N. P., G. Ayers, D. I. August, H. K. Cho, S. Kanev, C. Kozyrakis, T. Krishnamurthy, H. Litz, T. Moseley, and P. Ranganathan (2020). AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers. *IEEE Micro* **40**(3), 56–63.
3. Litz, H., R. J. Dias, and D. Cheriton (2015). Efficient Correction of Anomalies in Snapshot Isolation Transactions. *ACM Transactions on Architecture and Code Optimization (TACO)*.

Refereed Conference Papers

1. Chakraborttii, C. and H. Litz (2021). Reducing write amplification in flash by death-time prediction of logical block addresses. In: *Proceedings of the 14th ACM International Conference on Systems and Storage (SYSTOR)*, pp.1–12.
2. Kargar, S., H. Litz, and F. Nawab (2021). Predict and Write: Using K-Means Clustering to Extend the Lifetime of NVM Storage. In: *Proceedings of the 37th IEEE International Conference on Data Engineering (ICDE)*.
3. Chakraborttii, C. and H. Litz (2020a). Improving the accuracy, adaptability, and interpretability of SSD failure prediction models. In: *Proceedings of the 11th ACM Symposium on Cloud Computing (SoCC)*, pp.120–133.
4. Chakraborttii, C. and H. Litz (2020b). Learning I/O Access Patterns to Improve Prefetching in SSDs. In: *Proceedings of the European Conference on Machine Learning (ECML-PKDD'20)*.

5. Grossman, S., H. Litz, and C. Kozyrakis (2018). Making pull-based graph processing performant. In: *Proceedings of the 23rd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*.
6. Hashemi, M., K. Swersky, J. Smith, G. Ayers, H. Litz, J. Chang, C. Kozyrakis, and P. Ranganathan (2018). Learning Memory Access Patterns. In: *Proceedings of the 35th International Conference on Machine Learning (ICML)*.
7. Klimovic, A., H. Litz, and C. Kozyrakis (2018c). Selecta: Learning Heterogeneous Cloud Storage Configuration for Data Analytics. In: *Proceedings of the USENIX Annual Technical Conference (USENIX'18)*.
8. Litz, H., B. Braun, and D. R. Cheriton (2016). EXCITE-VM: Extending the Virtual Memory System to Support Snapshot Isolation Transactions. In: *25th International Confernce on Parallel Architectures and Compilation Techniques (PACT'25)*.
9. Fröning, H., M. Nüssle, H. Litz, C. Leber, and U. Brüning (2013). On achieving high message rates. In: *13th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid'13)*.
10. Leber, C., B. Geib, and H. Litz (2011). High Frequency Trading Acceleration using FPGAs. In: *21st International Conference on Field Programmable Logic and Applications (FPL'21)*.
11. Fröning, H., M. Nüssle, H. Litz, and U. Brüning (2010). A Case for FPGA based Accelerated Communication. In: *9th International Conference on Networking (ICN'9)*.
12. Litz, H., M. Thürmer, and U. Brüning (2010). TCCluster: A Cluster Architecture Utilizing the Processor Host Interface as a Network Interconnect. In: *2010 IEEE International Conference on Cluster Computing (CLUSTER)*.
13. Fröning, H., H. Litz, and U. Brüning (2009). Efficient Virtualization of High-Performance Network Interfaces. In: *8th International Conference on Networks (ICN'8)*.
14. Litz, H., H. Froning, M. Thürmer, and U. Brüning (2009). An FPGA based Verification Platform for HyperTransport 3.x. In: *19th International Conference on Field Programmable Logic and Applications (FPL'19)*.
15. Litz, H., H. Fröning, M. Nüssle, and U. Brüning (2008). VELO: A Novel Communication Engine for Ultra-low Latency Message Transfers. In: *37th International Conference on Parallel Processing (ICPP'08)*.
16. Fröning, H., M. Nüssle, D. Slogsnat, H. Litz, and U. Brüning (2006). The HTX-Board: A Rapid Prototyping Station. In: *3rd annual FPGAWorld Conference*.
17. Ding, Y. and H. Litz (2005). Creating Multiplatform User Interfaces by Annotation and Adaption. In: *11th International Conference on Intelligent User Interfaces (IUI'11)*.
18. Ding, Y., H. Litz, and D. Pfisterer (2004). A graphical single-authoring framework for building multi-platform user interfaces. In: *9th international conference on Intelligent user interface (IUI'9)*.

Refereed Workshop Papers

1. Klimovic, A., H. Litz, and C. Kozyrakis (2018a). Learning Heterogeneous Cloud Storage Configuration for Data Analytics. In: *SysML Conference*.
2. Klimovic, A., H. Litz, and C. Kozyrakis (2018b). ReFlex: Remote Flash == Local Flash. In: *9th Annual Non-Volatile Memories Workshop*.
3. Wang, B., H. Litz, and D. R. Cheriton (2014). HICAMP bitmap: space-efficient updatable bitmap index for in-memory databases. In: *10th International Workshop on Data Management on New Hardware (DAMON'10)*.
4. Chan, M., H. Litz, and D. R. Cheriton (2013). Rethinking network stack design with memory snapshots. In: *14th USENIX Conference on Hot Topics in Operating Systems (HotOs'14)*.
5. Litz, H., C. Leber, and B. Geib (Nov. 2011). DSL Programmable Engine for High Frequency Trading Acceleration. In: *4th Workshop on High Performance Computational Finance (WHPCF '11)*.

6. Froning, H. and H. Litz (2010). Efficient hardware support for the partitioned global address space. In: *24th IEEE International Symposium on Parallel & Distributed Processing, Workshops and Phd Forum (IPDPSW)*,
7. Litz, H., H. Fröning, and U. Brüning (2010). HTAX: A Novel Framework for Flexible and High Performance Networks-on-Chip. In: *4th Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC'4)*.
8. Kalisch, B., A. Giese, H. Litz, and U. Brüning (2009). HyperTransport 3 Core: A Next Generation Host Interface with Extremely High Bandwidth. In: *1st International Workshop on HyperTransport Research and Applications (WHTRA'09)*.
9. Litz, H., H. Fröning, and U. Brüning (2009). A HyperTransport 3 Physical Layer Interface for FPGAs. In: *6th International Symposium on Applied Reconfigurable Computing (ARC'6)*.

Patents

Benjamin Geib, Heiner Litz, Mondrian Nuessle. "Circuit arrangement for connection interface". DE102011009518B4, EP2668763A2, US20140207881, filed 2011, assigned 2014.

Grants

I have acquired as PI or Co-PI $2,9 million in external research grants since 2017.

2021	H. Litz "Google gift"	$60,000
2021	H. Litz "Facebook gift"	$60,000
2020	H. Litz "NSF CAREER award"	$529,995
2020	D. Long and H. Litz "NSF IUCRC Phase II grant"	$500,000
2020	H. Litz "Samsung gift"	$70,000
2020	H. Litz "Samsung research contract"	$120,000
2020	R. Sanfelice, H. Litz, A. Halder "UCSC center-scale seed funding award"	$75,000
2018	H. Litz and B. Paten "Accelerating Genomics Workloads with Smart SSDs". WD	$960,000
2018	H. Litz "FoMR: Improving Microprocessor IPC for Data Center Workloads". NSF/Intel	$360,000
2018	H. Litz and R. Felice "Optimized Trajectory planning for Automotive Vehicles", NXP	$50,000
2017	H. Litz "NVMe Device Level support for Quality of Service". Samsung	$100,000
2017	H. Litz "Data Center Flash Storage Disaggregation". Broadcom	$100,000

Service

ASPLOS'23	Extended Technical Program Comittee
NVMW'22	Technical Program Comittee
Eurosys'22	Technical Program Comittee
ISCA'22	Technical Program Comittee
MICRO'21	Technical Program Comittee
ISCA'21	Technical Program Comittee
MICRO'20	Technical Program Comittee
Usenix ATC'21	Technical Program Comittee
IEEE MICRO	Editor
Systor'20	Technical Program Comittee
Usenix ATC'20	Technical Program Comittee
SOCC'19	Technical Program Comittee
MICRO'19	Technical Program Comittee
HotOS'19	Technical Program Comittee
ISCA'19	External Technical Program Comittee
DoE	Panelist Basic Research Needs for Microelectronics
HPCA-IS'19	Technical Program Committee
PPoPP'19	Technical Program Committee
SOCC'18	Technical Program Committee
Micro'17	External Technical Program Committee
TACO'16	Technical Program Committee
HPCA'15	External Technical Program Committee
ReCoSoC'11-16	Technical Program Committee
HUCAA'13-15	Technical Program Committee

Invited Talks

Data center Operating Systems

October 2020	Intel
August 2020	IBM
August 2020	Nutanix
August 2020	VMWare
October 2019	Intel
August 2019	Samsung
August 2019	VMWare
March 2019	Facebook
December 2018	IAP Industry Academia Partnership
August 2018	ITU University Kopenhagen
June 2018	Heidelberg University
June 2018	SAP, Walldorf
March 2017	UCSC
Dec 2016	Facebook
July 2016	Amazon AWS
July 2016	CNEX
July 2016	Google
July 2016	Cavium
Apr 2016	Ericsson
Feb 2016	Broadcom
Feb 2016	Stanford Platform Lab

Snapshot Isolation based Transactional Memory

Sep 2015 Samsung
July 2015 VMWare
July 2014 Heidelberg University
Jun 2013 HP Labs
Nov 2012 Stanford CIS

In Memory Deduplication

Nov 2013 SAP Labs
Oct 2013 High Performance Transaction Systems (HPTS)

High Frequency Trading with FPGAs

May 2012 Oracle Labs

HyperTransport Cache Coherent Interconnect and its Applications

Aug 2011 University of Valencia
Aug 2011 University of Albacete
Mar 2011 KLA-Tencor
Mar 2008 SUN Microsystems

Status

German citizen, with US Green Card